

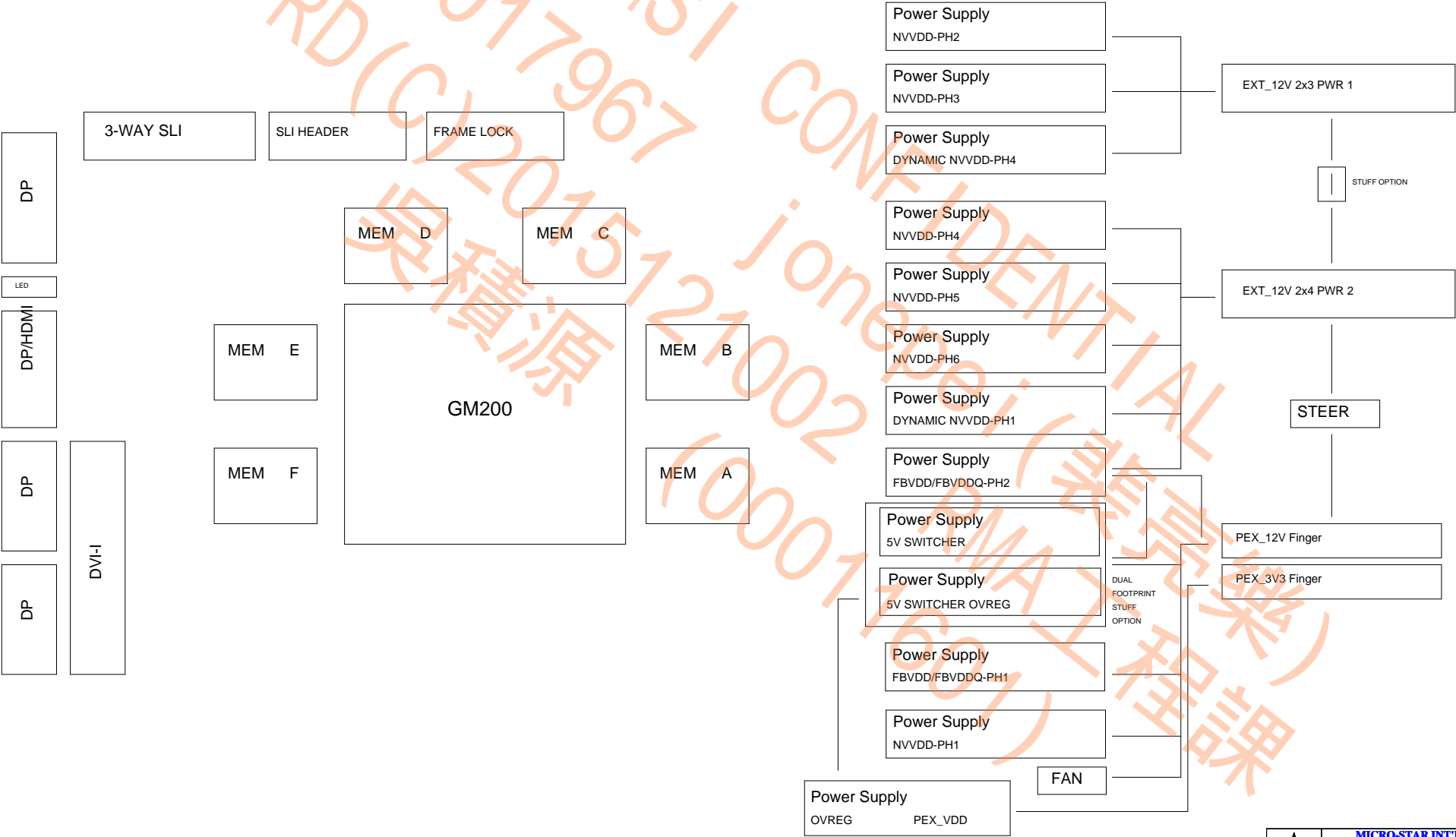
PG600-B02 NIGHTHAWK

GB3B-384, 6GB GDDR5 128Mx32

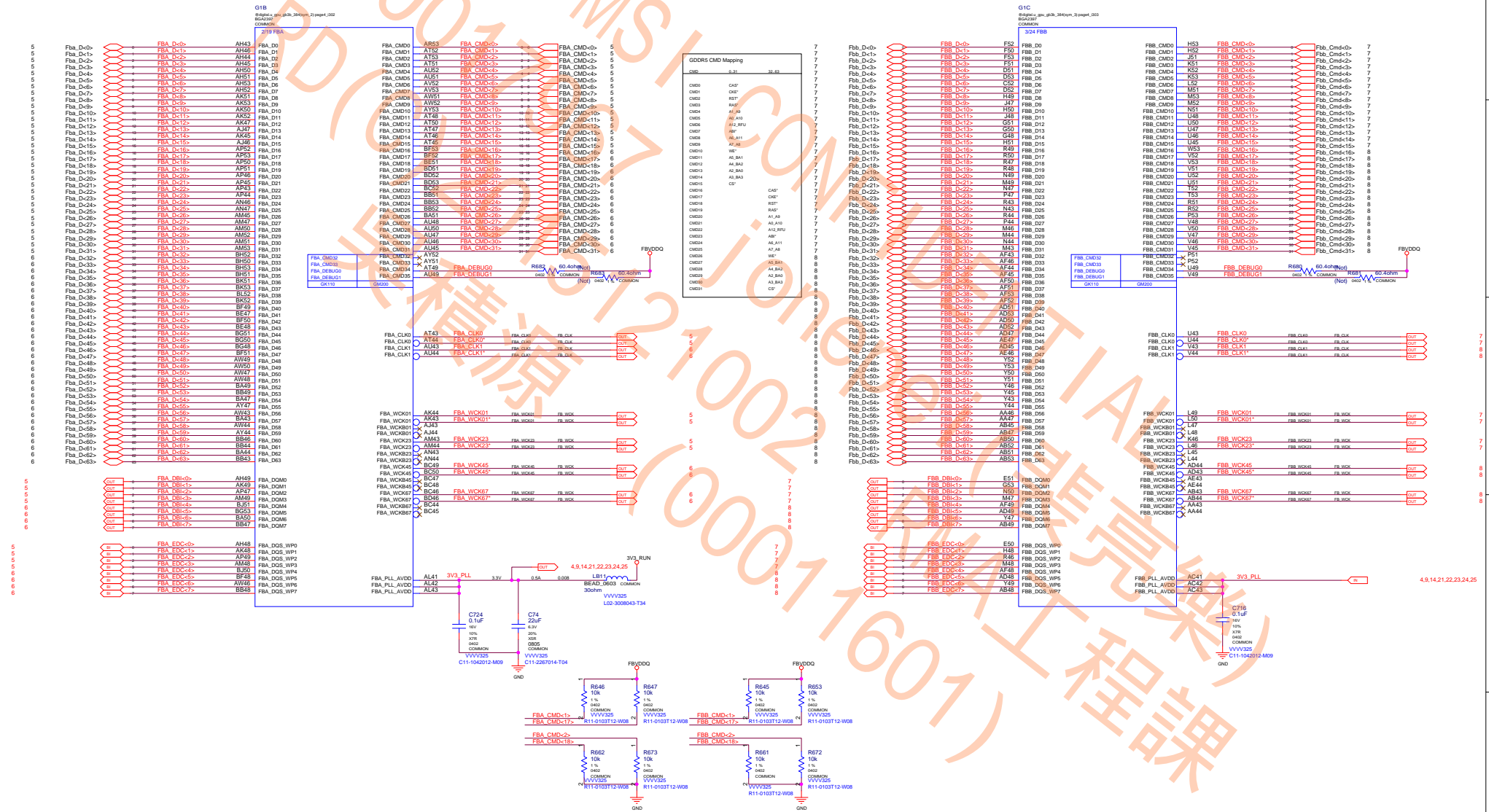
DP + HDMI/DP + DP + DP + DVI-I

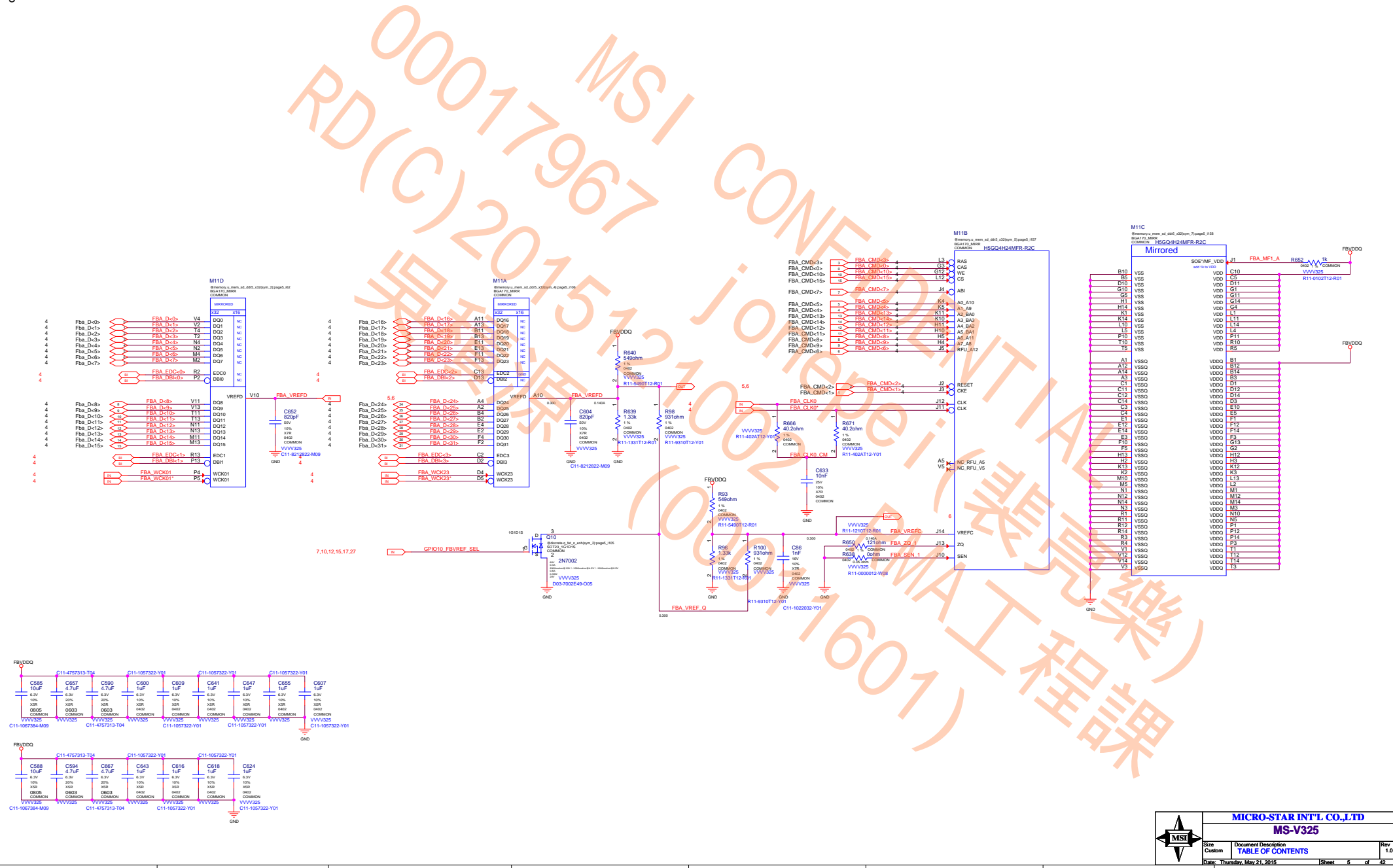
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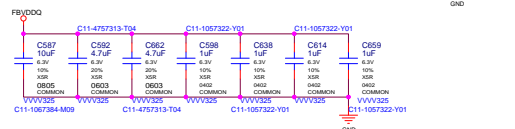
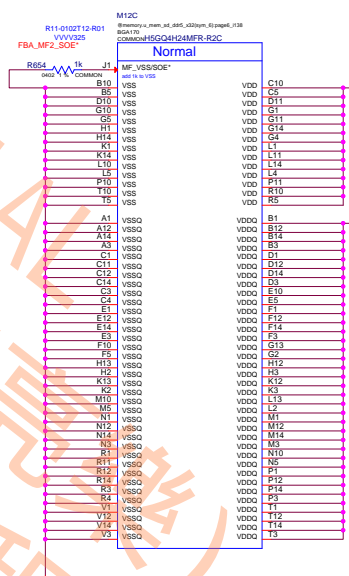
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11	MEMORY: FBC[63:32]	36	PS: Inputs, Filtering, and Monitoring
12	MEMORY: FBD[31:0]	37	PS: Shutdown
13	MEMORY: FBD[63:32]	38	PS: 12V Current Steering & Hot Unplug Detect
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19	GPU PWR and GND		
20	GPU Decoupling		
21	DACA Interface		
22	IFPAB DVI-I-DL		
23	IFPEF DP + DP		
24	IFPC HDMI / DP		
25	IFPD DP		

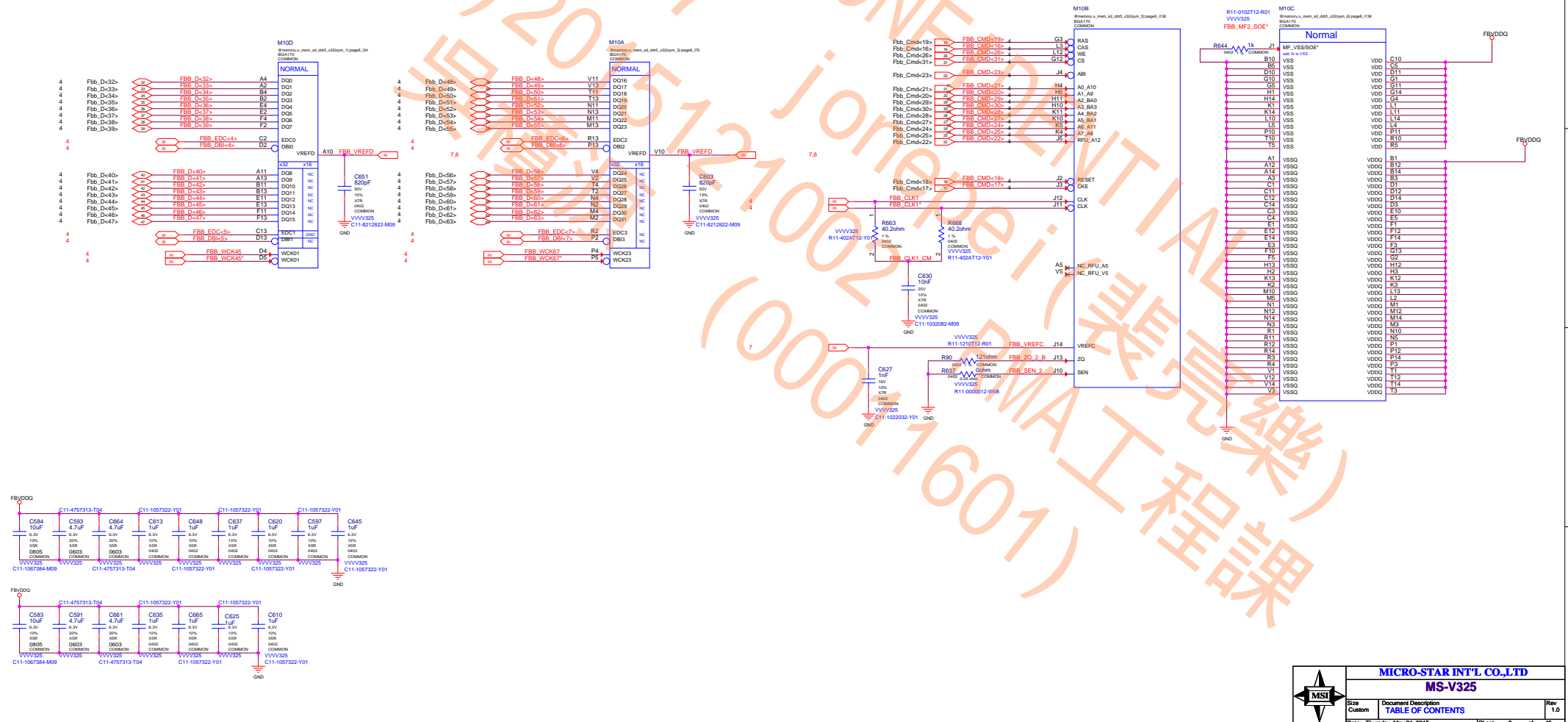


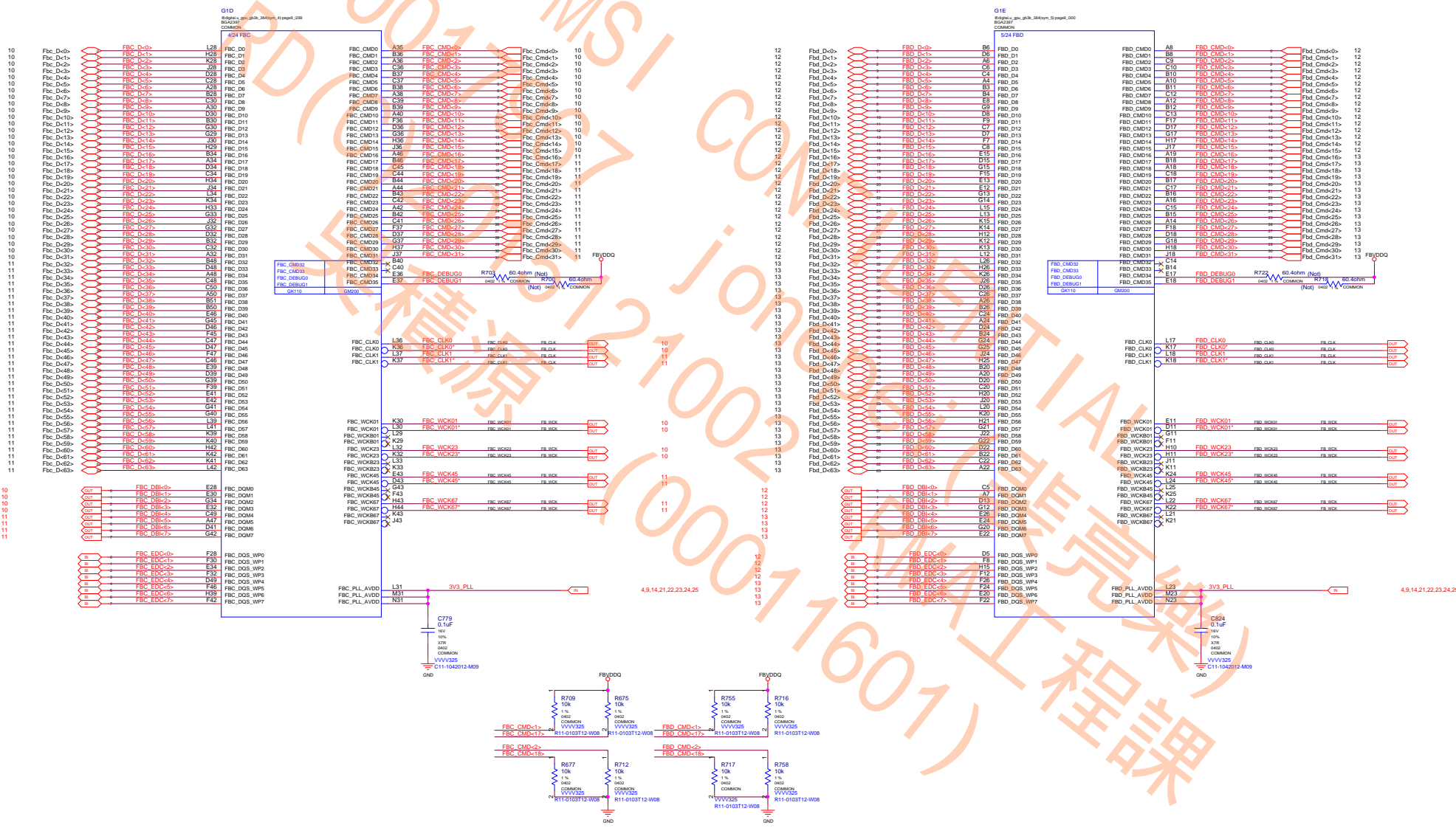


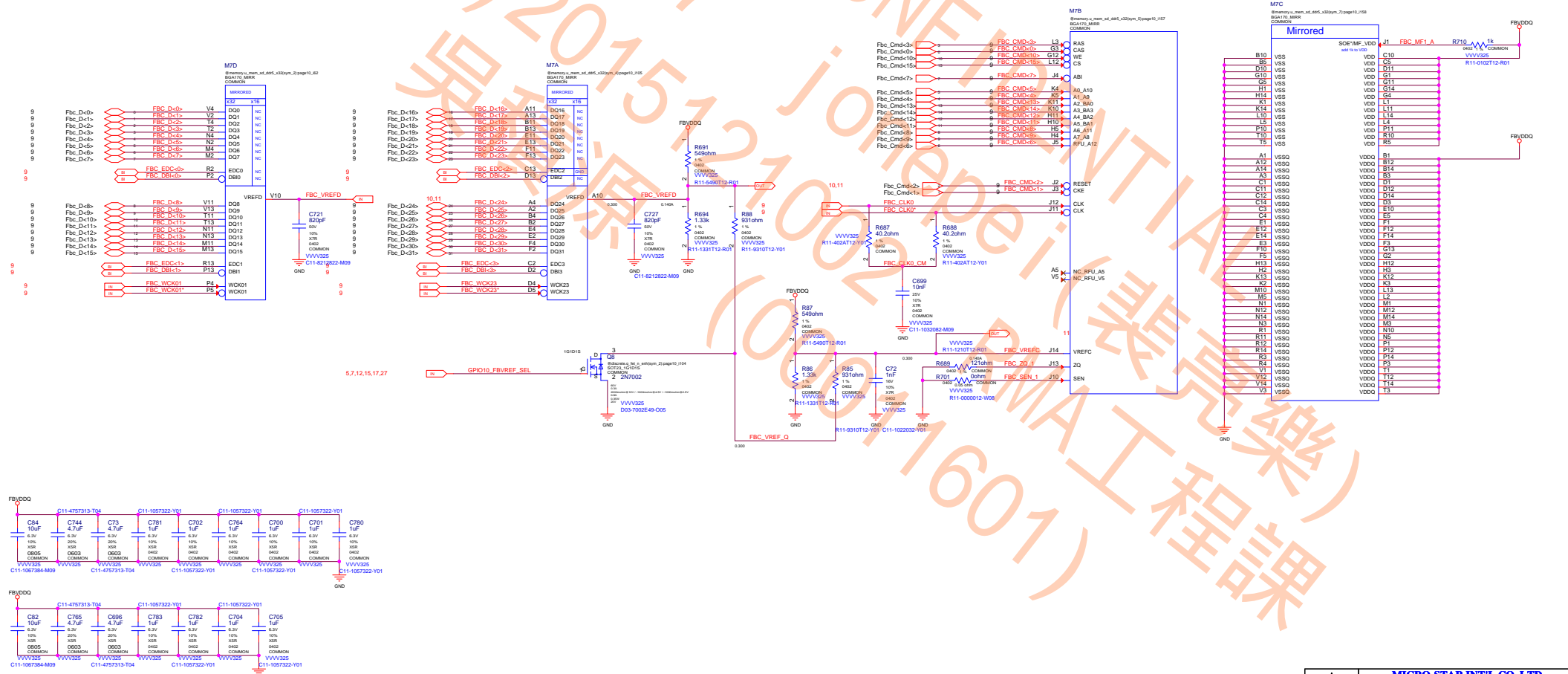


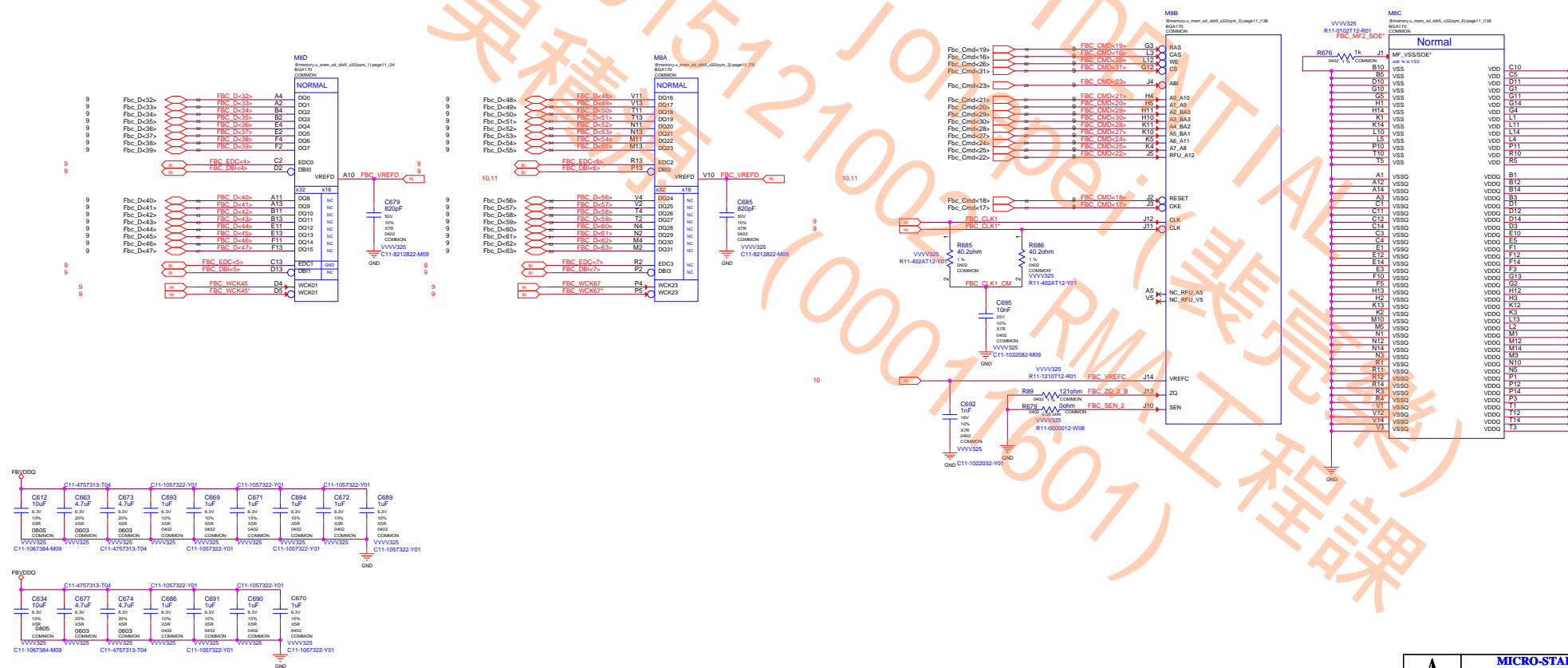


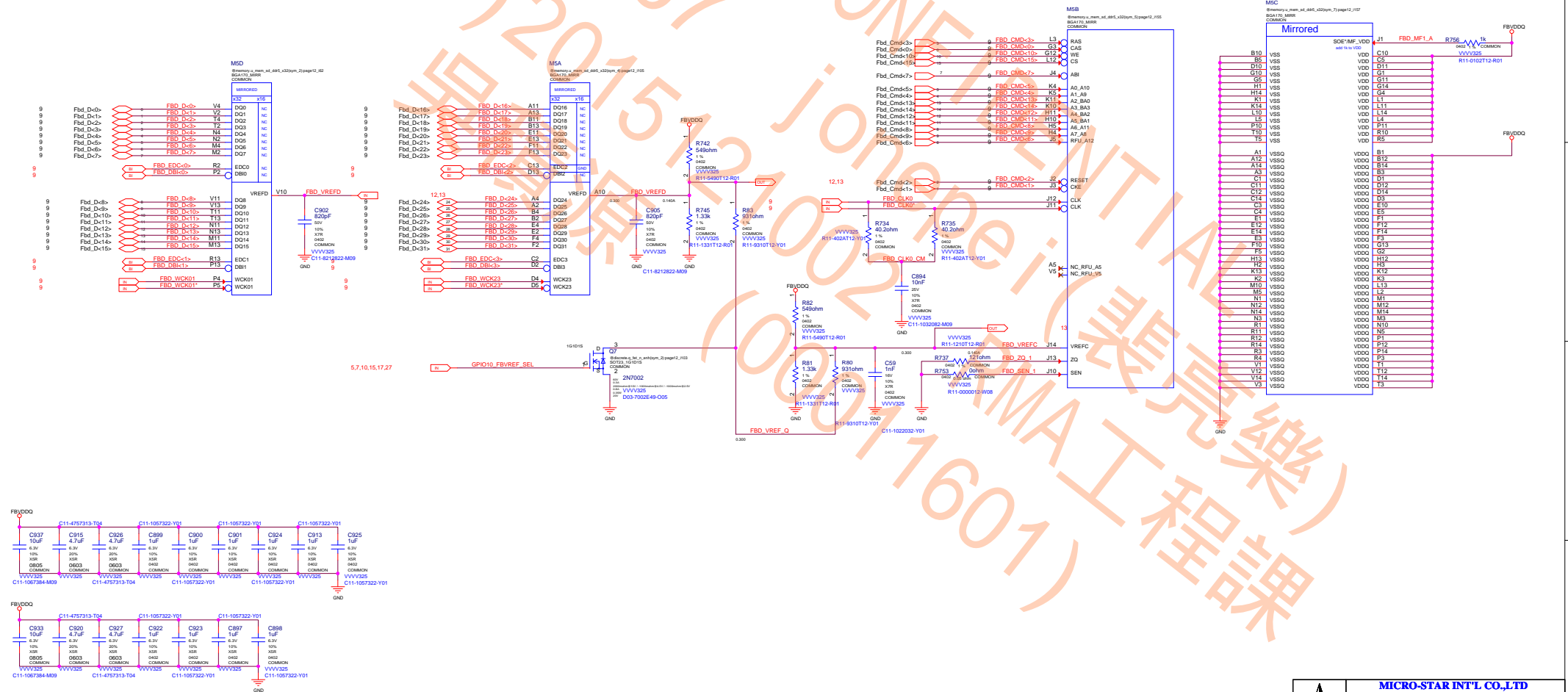


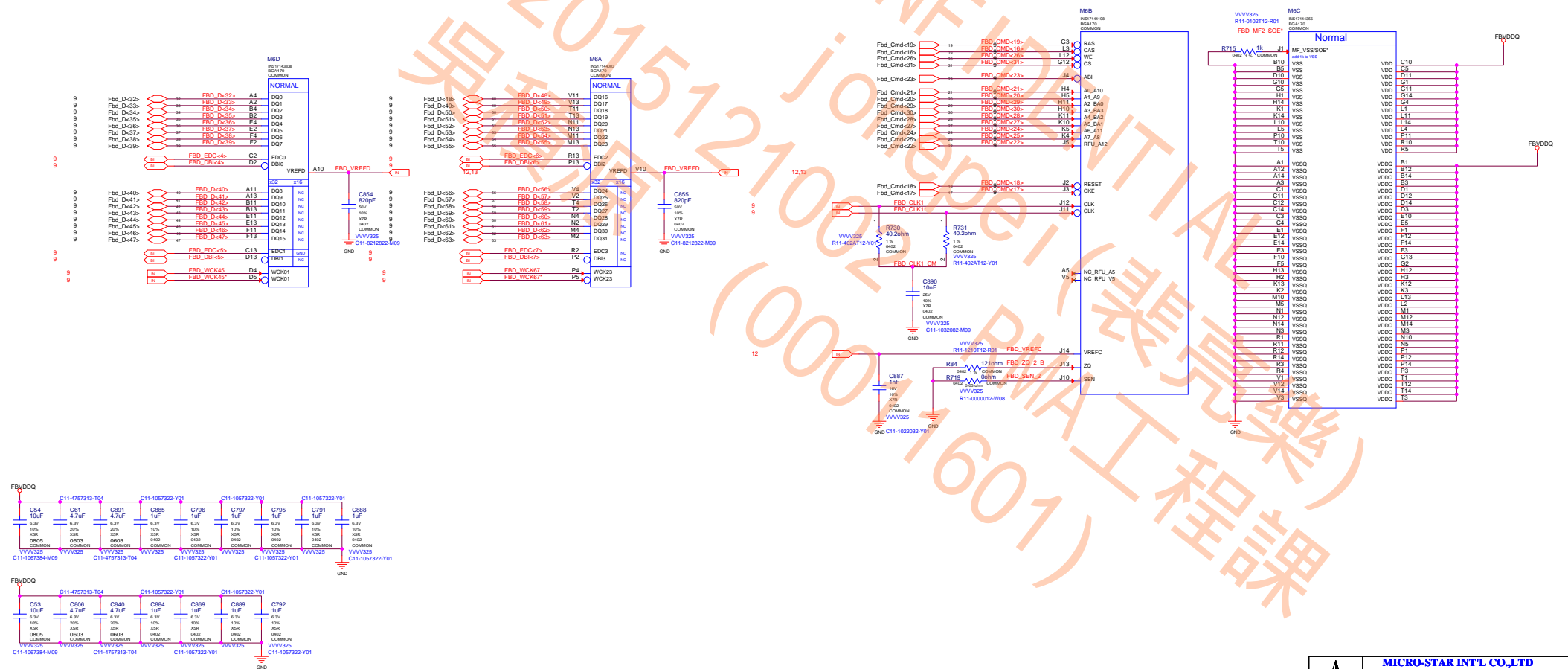




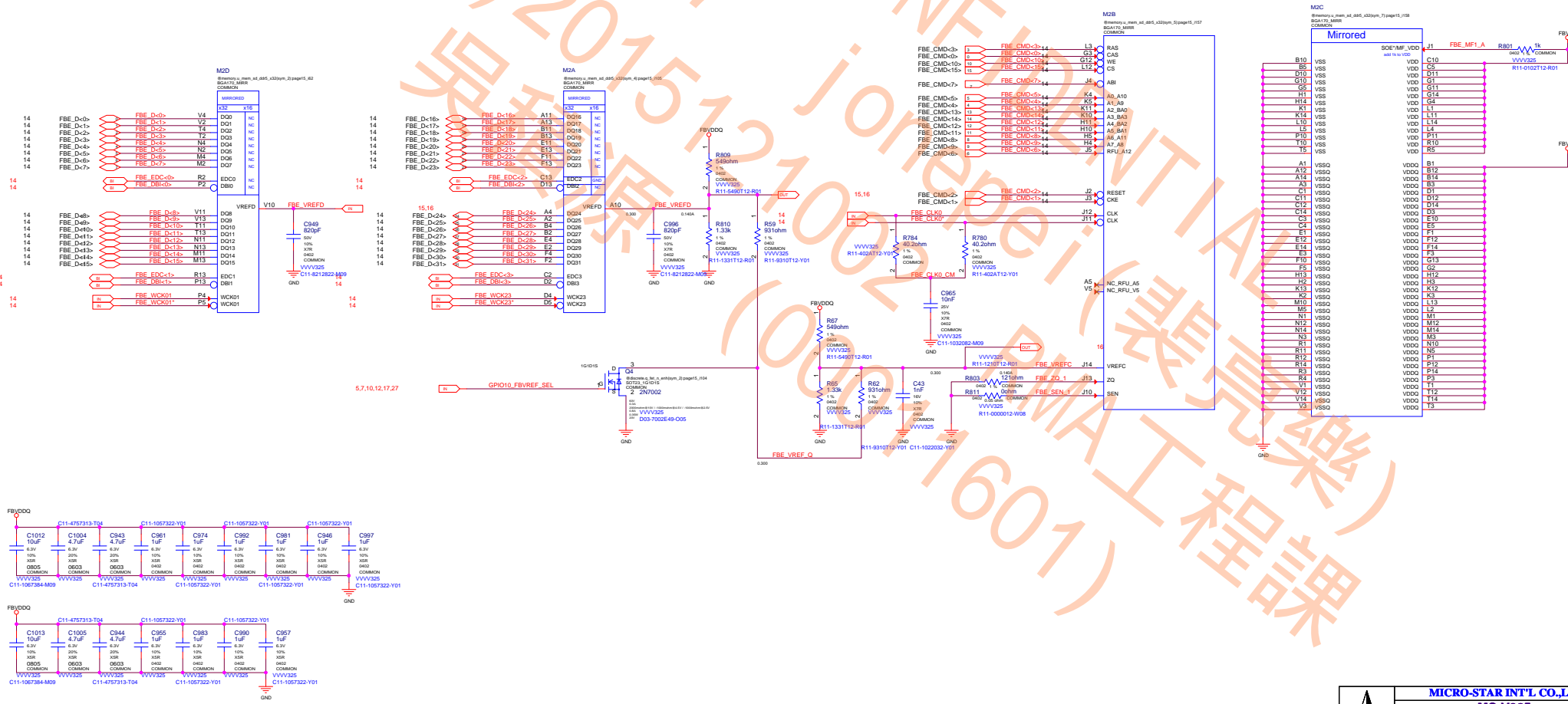


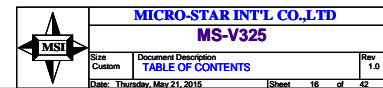


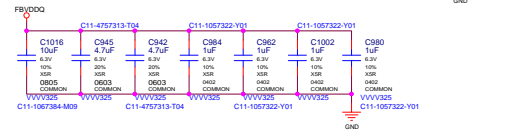
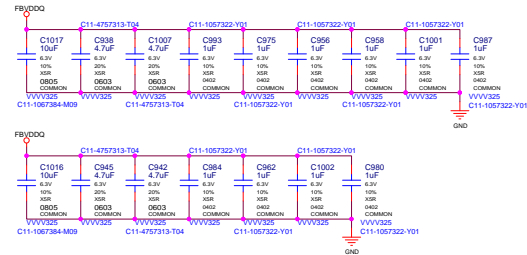


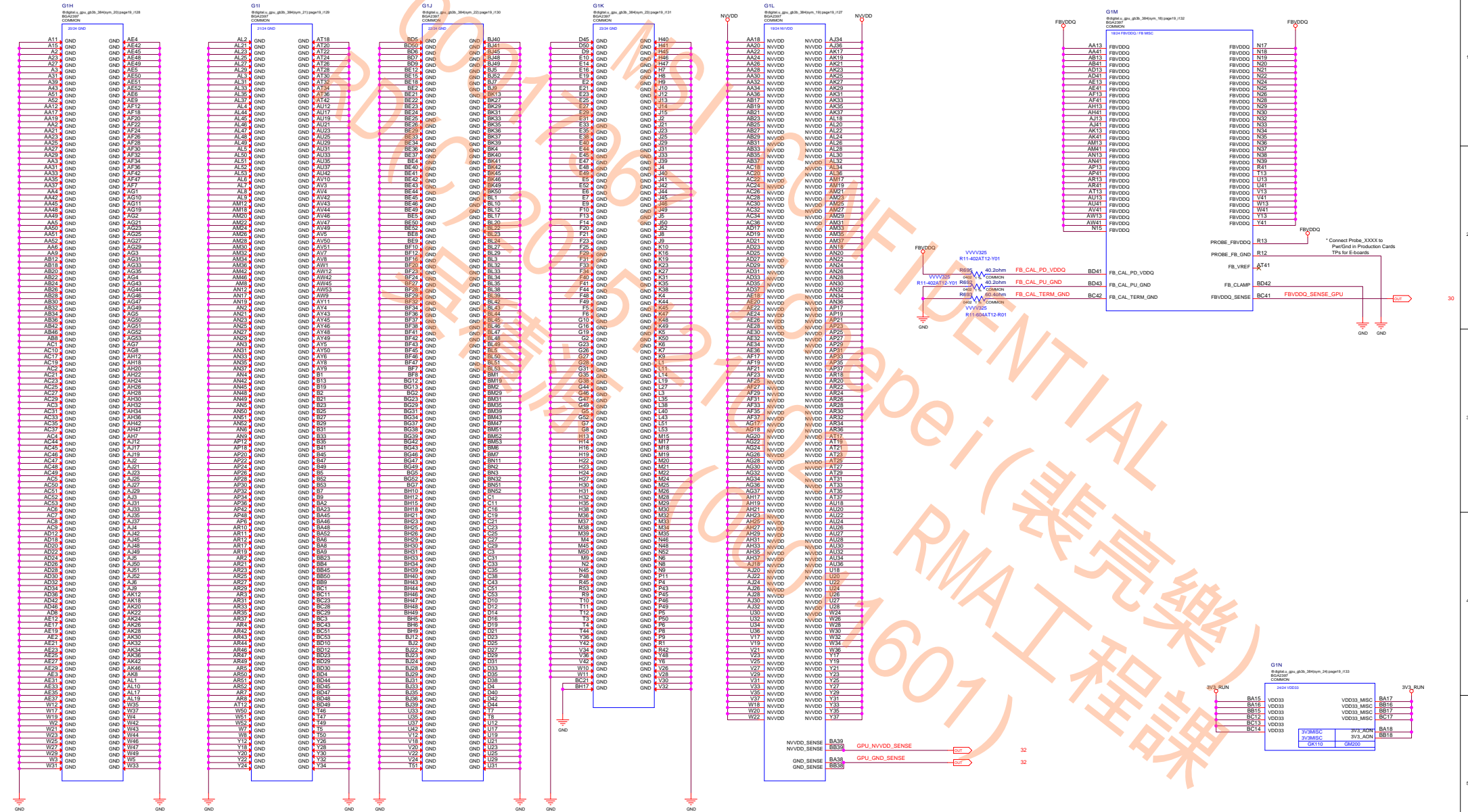




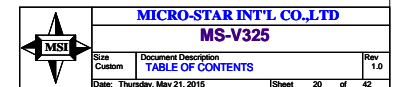
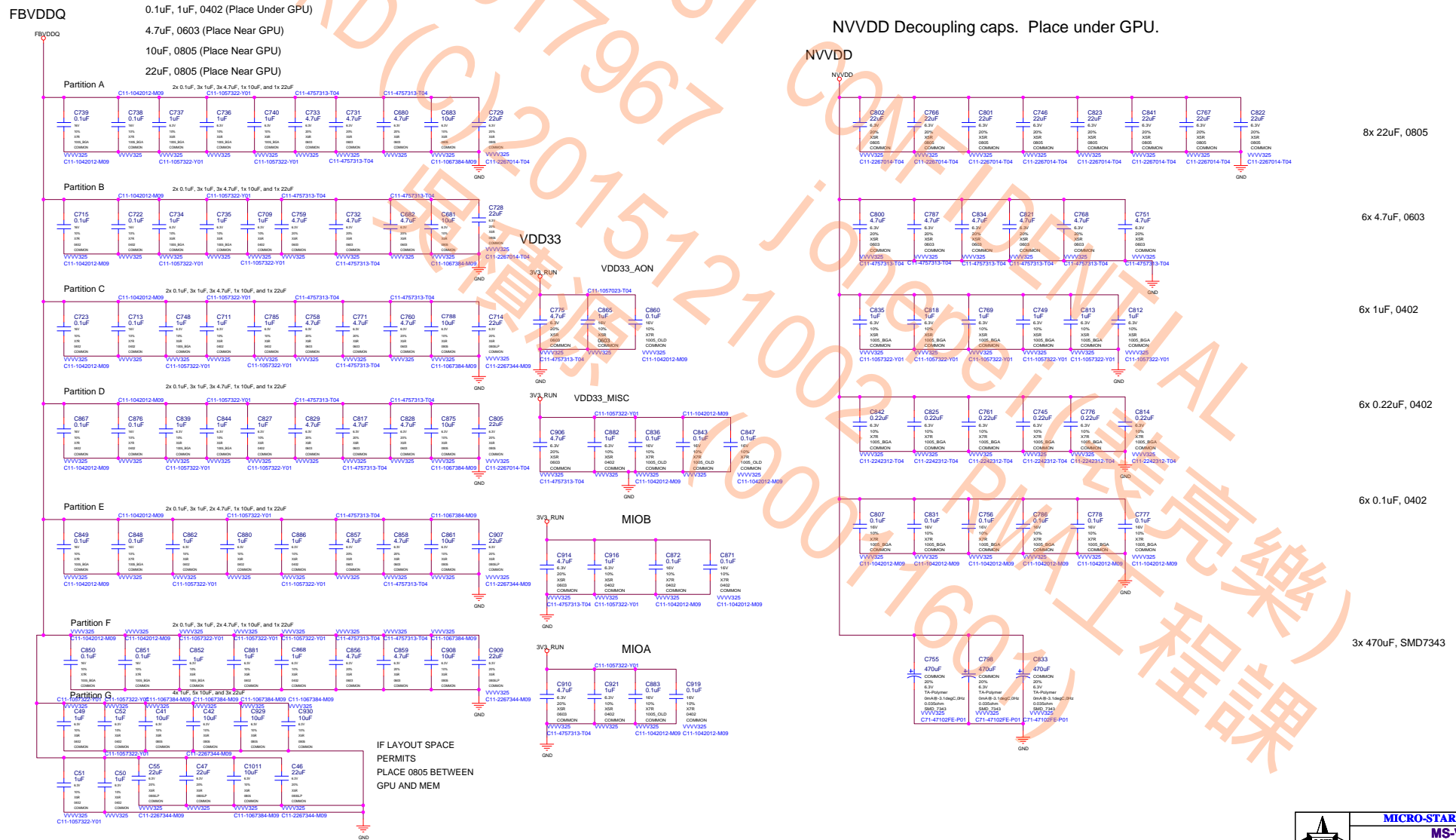


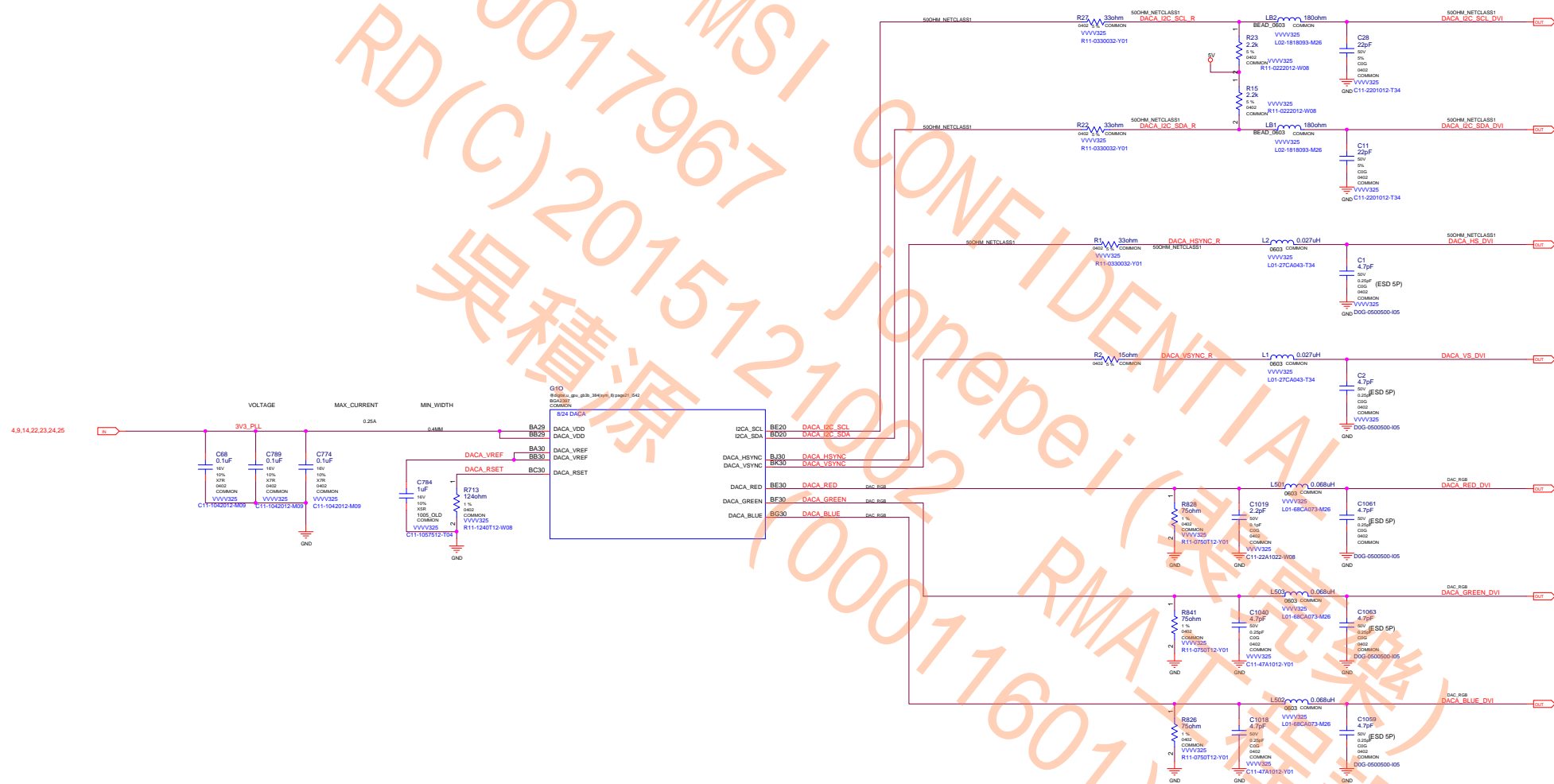




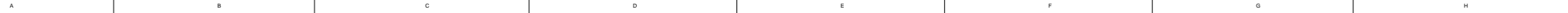


Based on GB3-X GDDR5 FBVDDQ Decap Guideline




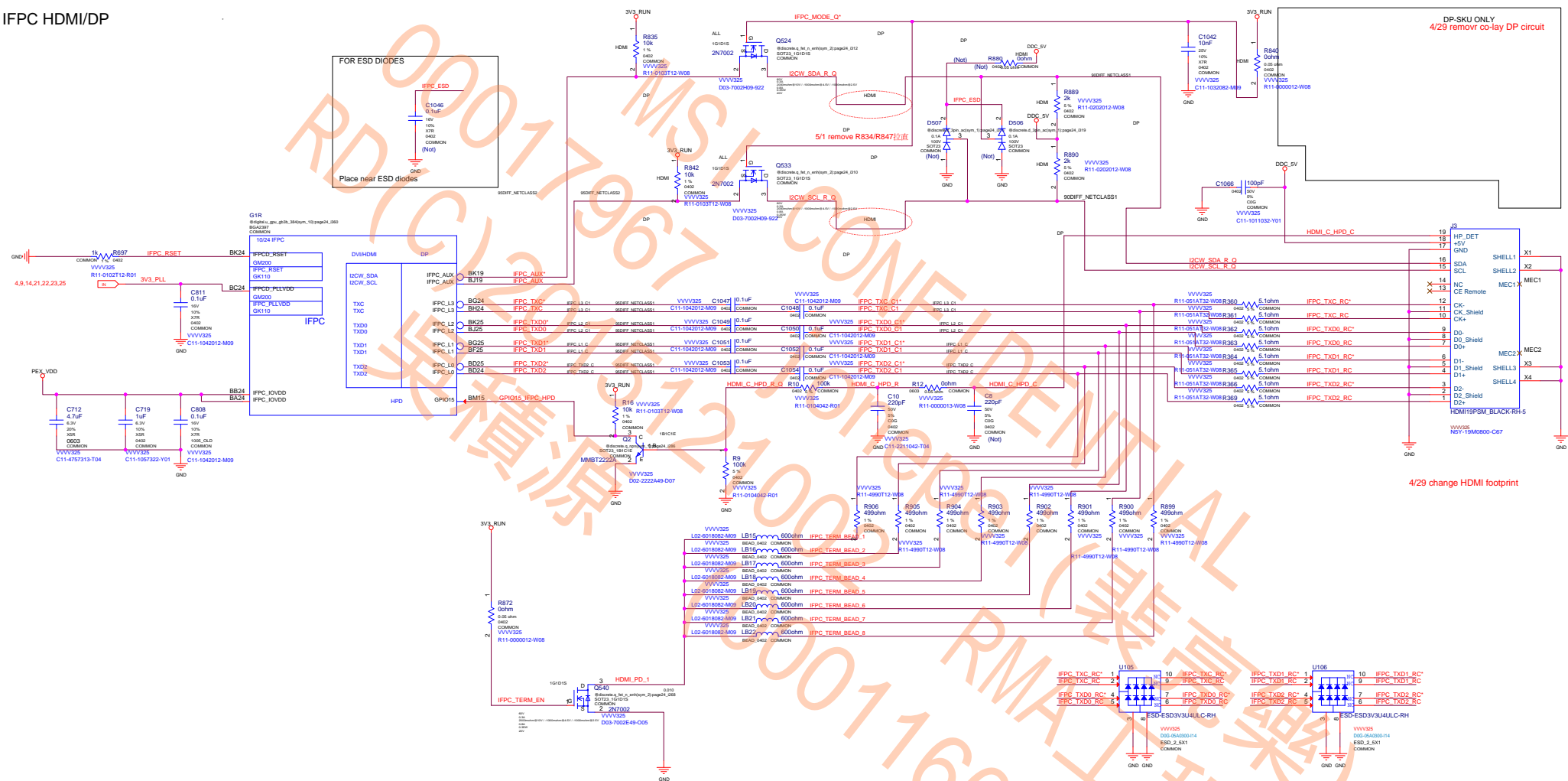


REPLACE WITH ZERO OHM RESISTORS FOR KEPLER SKUs

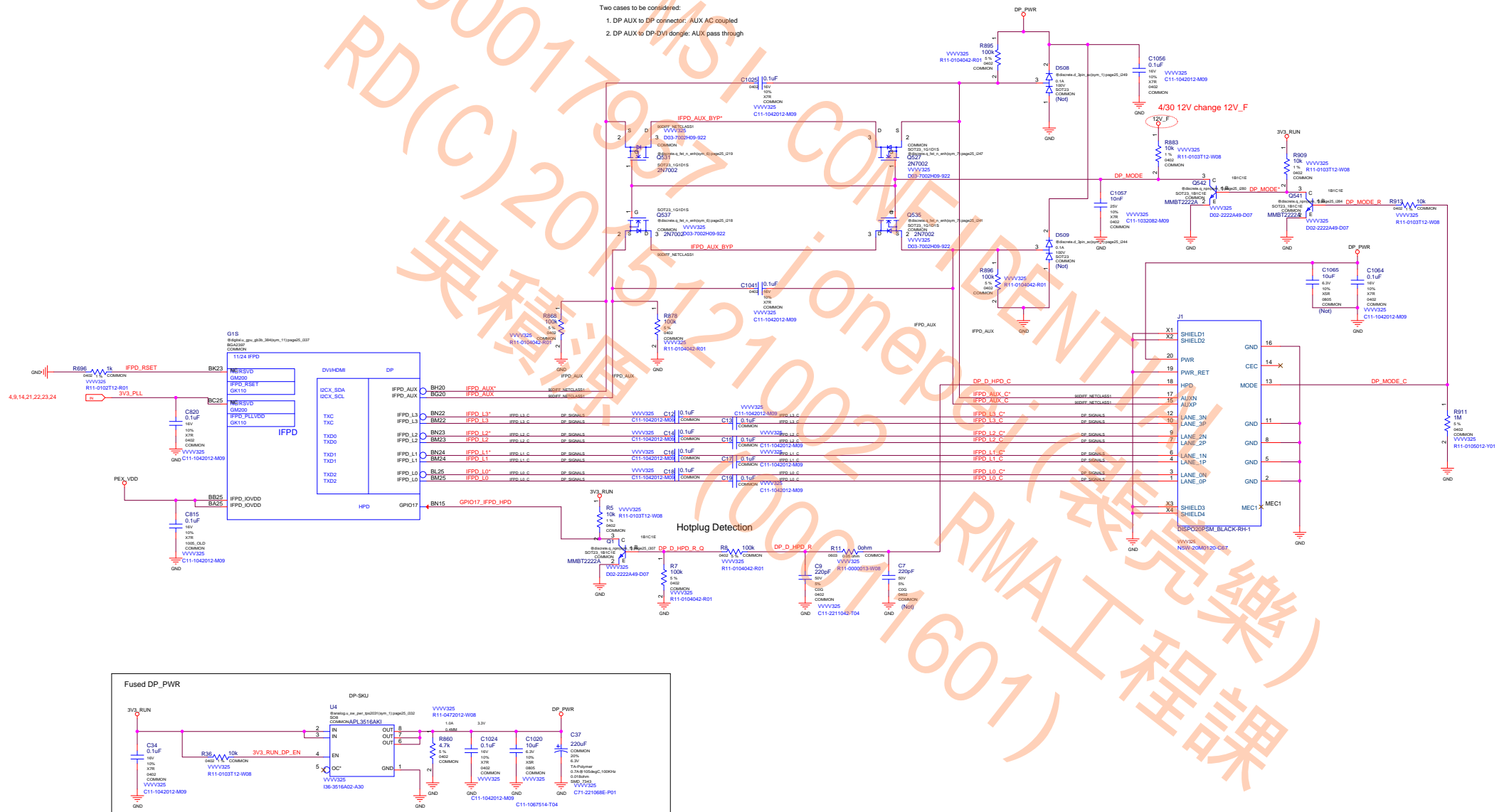





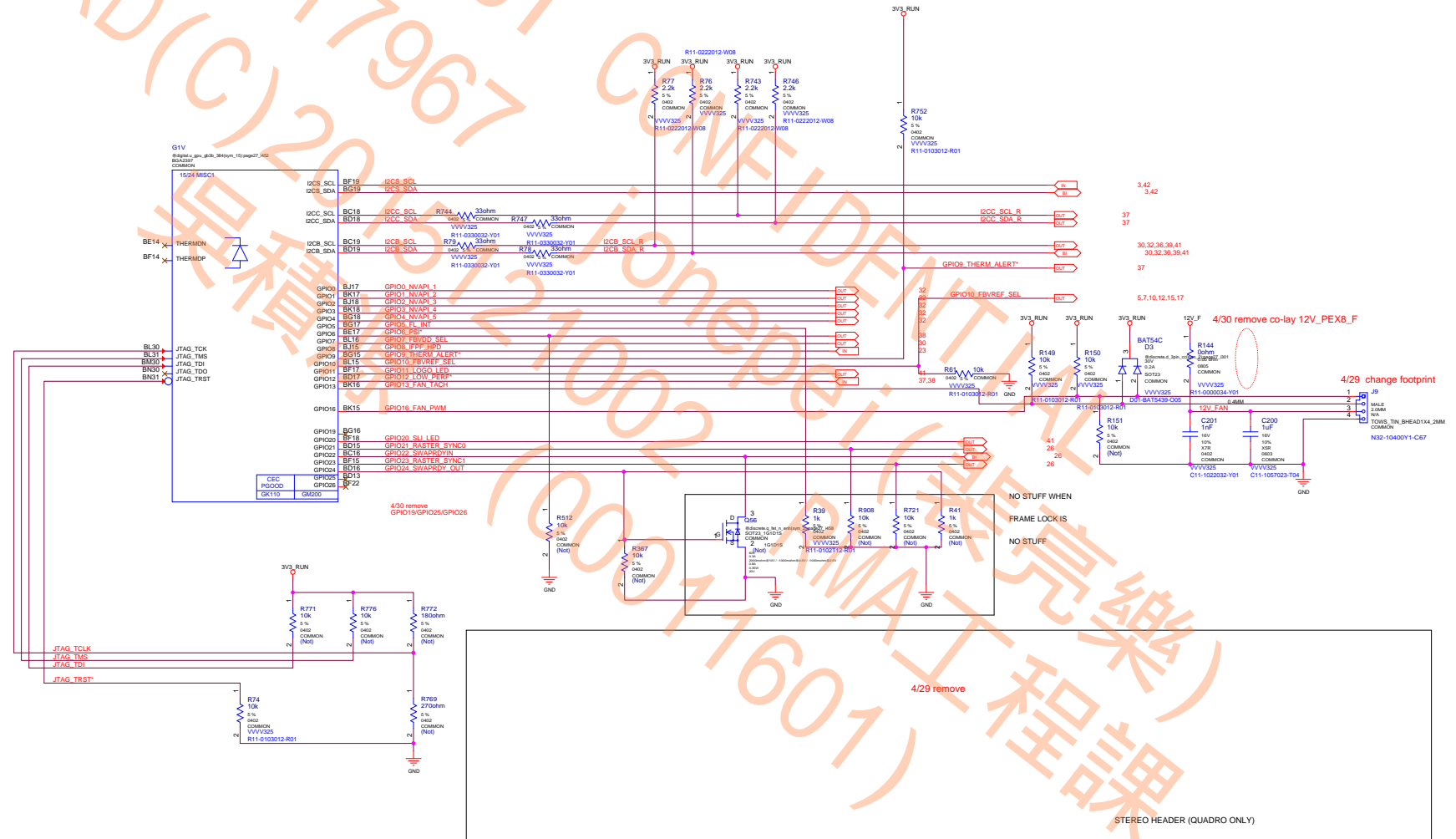
	MICRO-STAR INT'L CO.,LTD		
	MS-V325		
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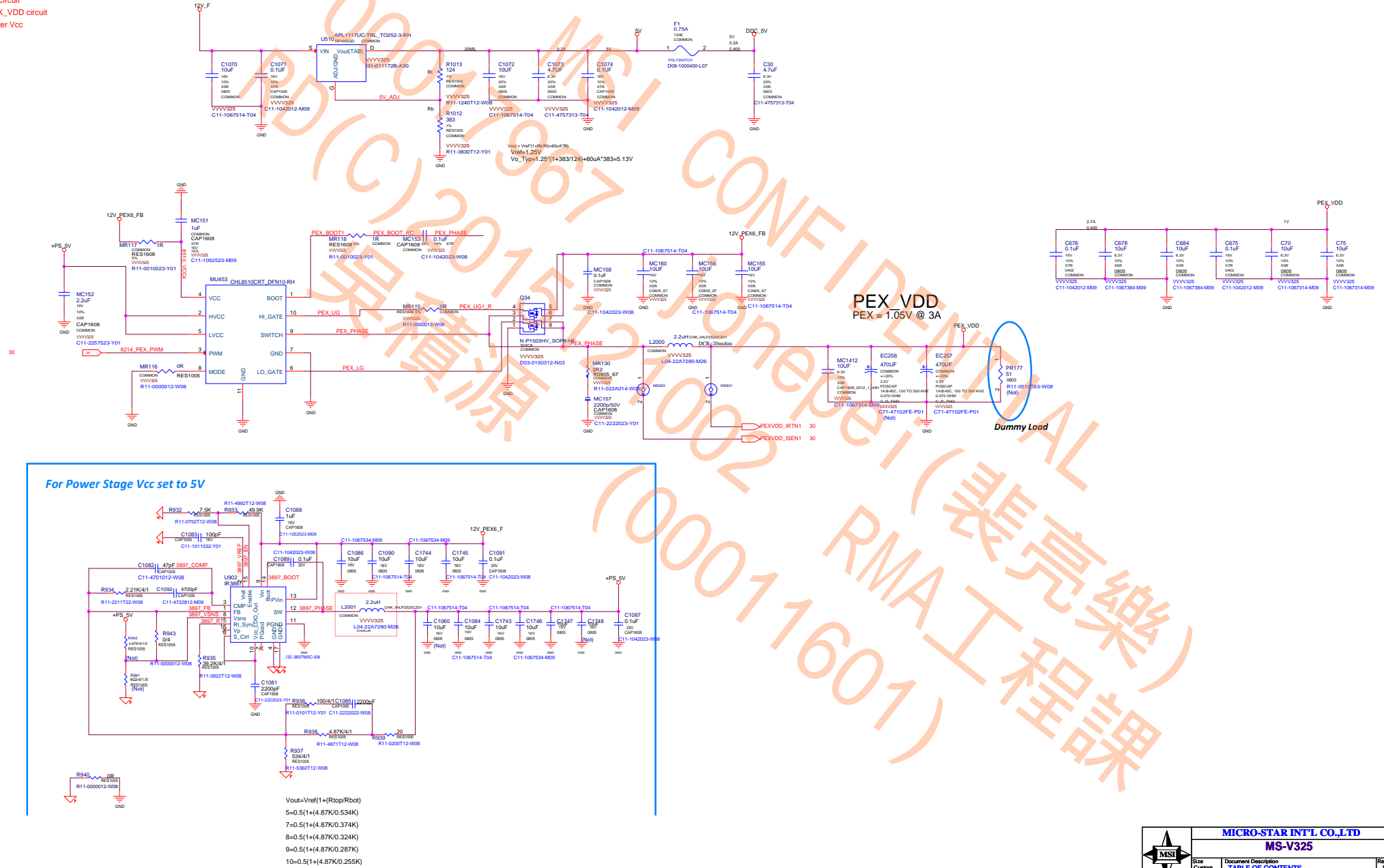
- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

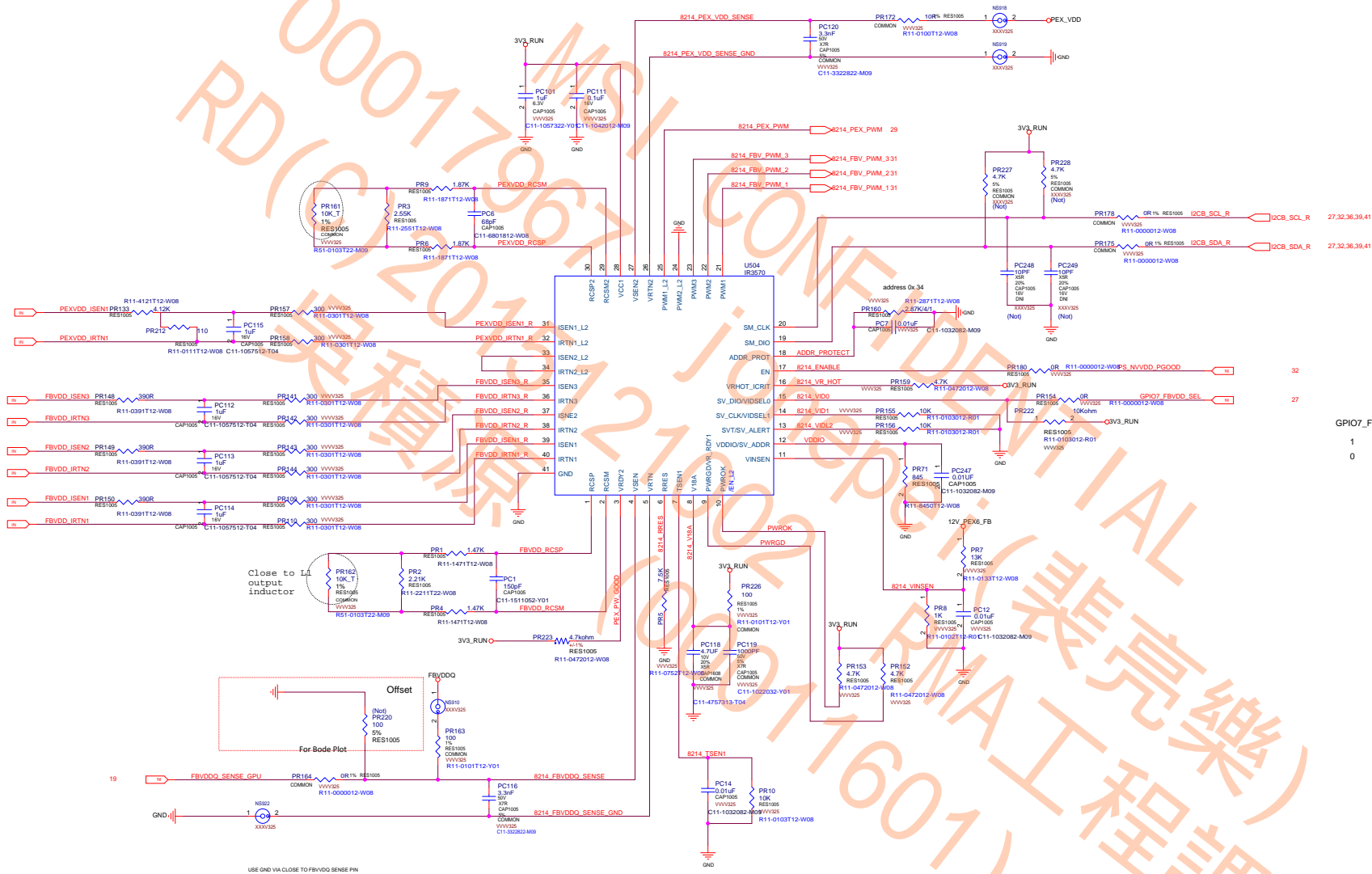


	MICRO-STAR INT'L CO.,LTD MS-V325		
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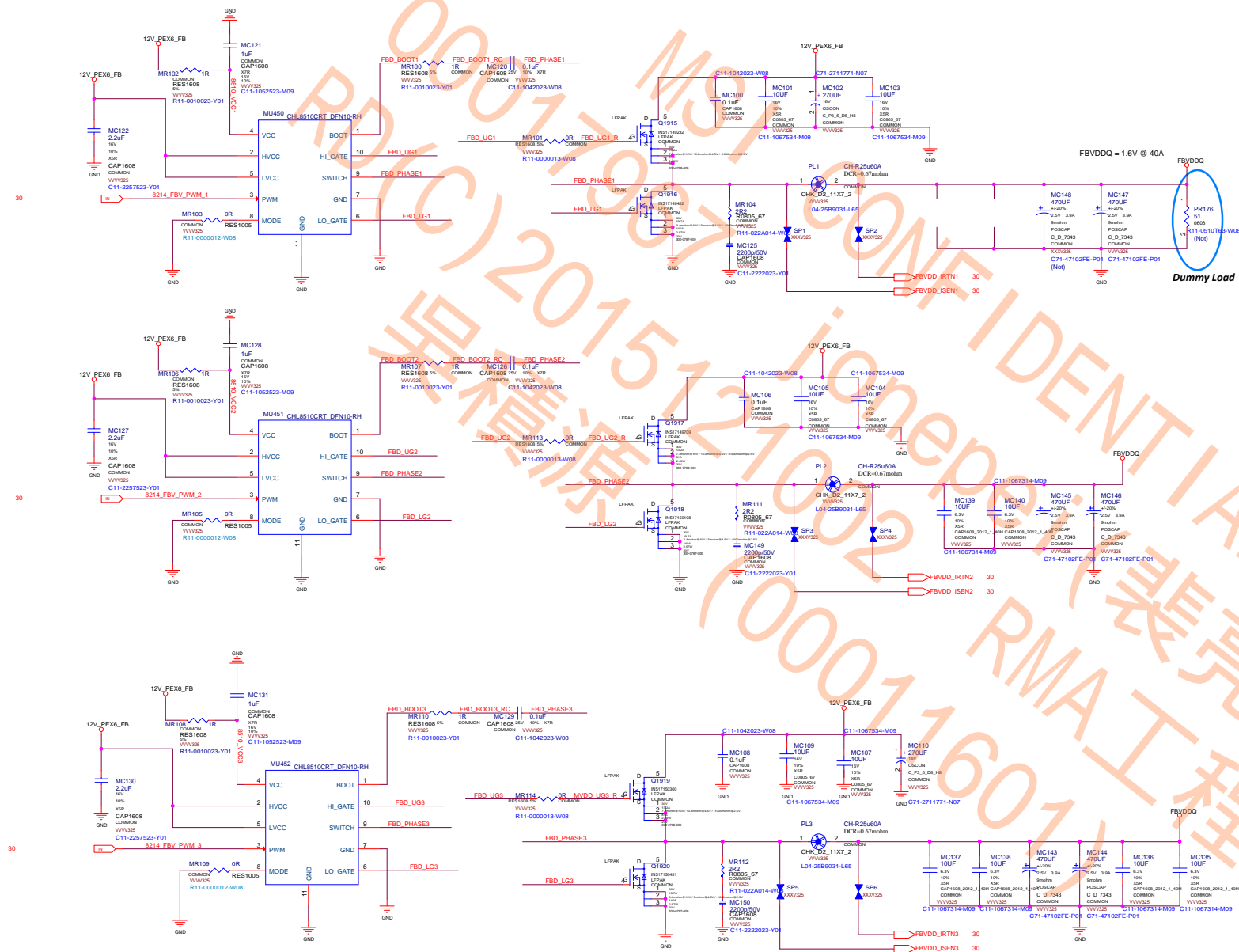


4/27 change 5V circuit
4/29 change PEX_VDD circuit
4/29 add 5V Driver Vcc



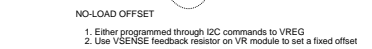


GPIO7_FBVDD_SEL	VOUT
1	1.56V
0	1.35V



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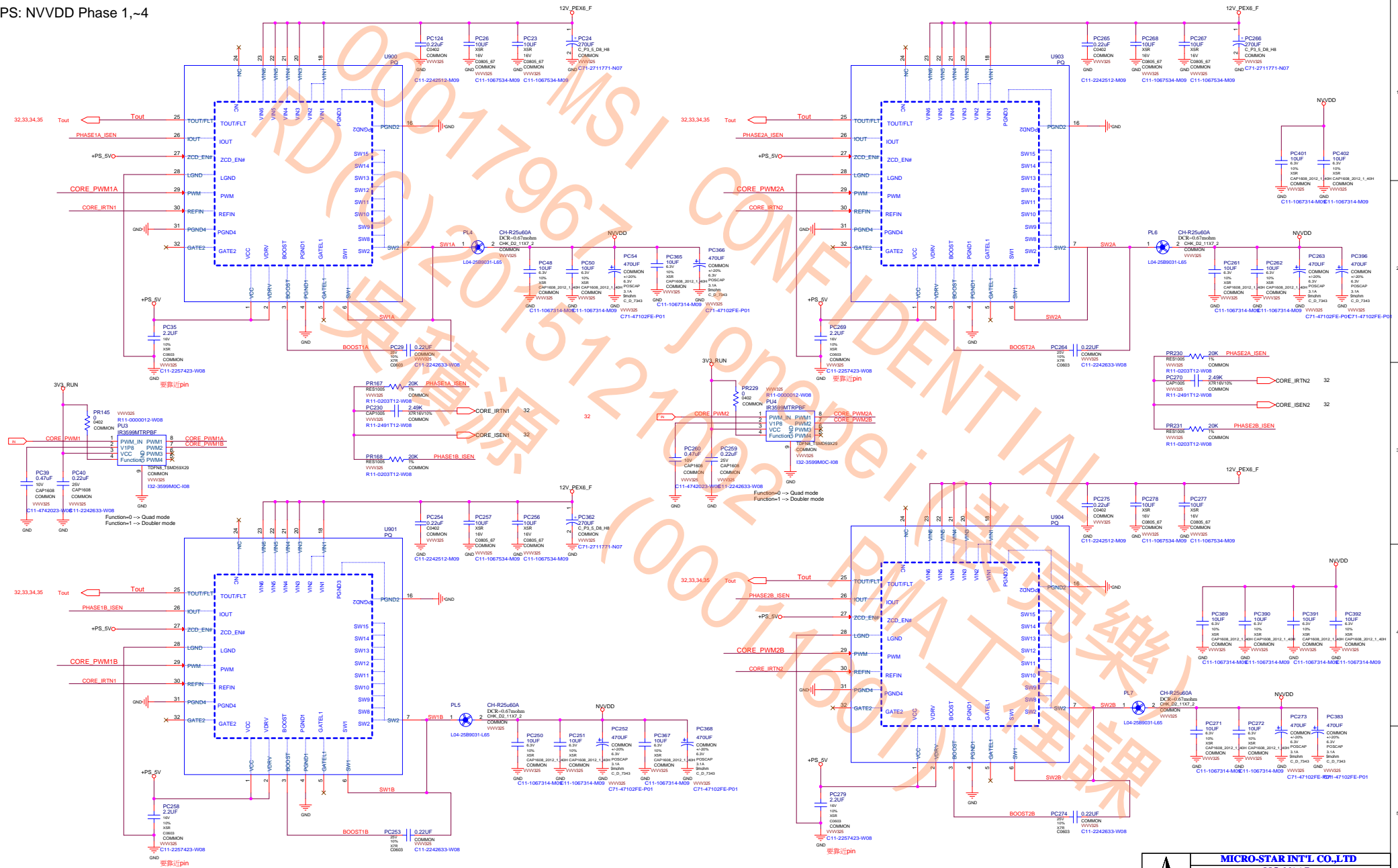


SOFT START (VR11)

1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170µS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
VID[5:1]=11001 to set 0.9V

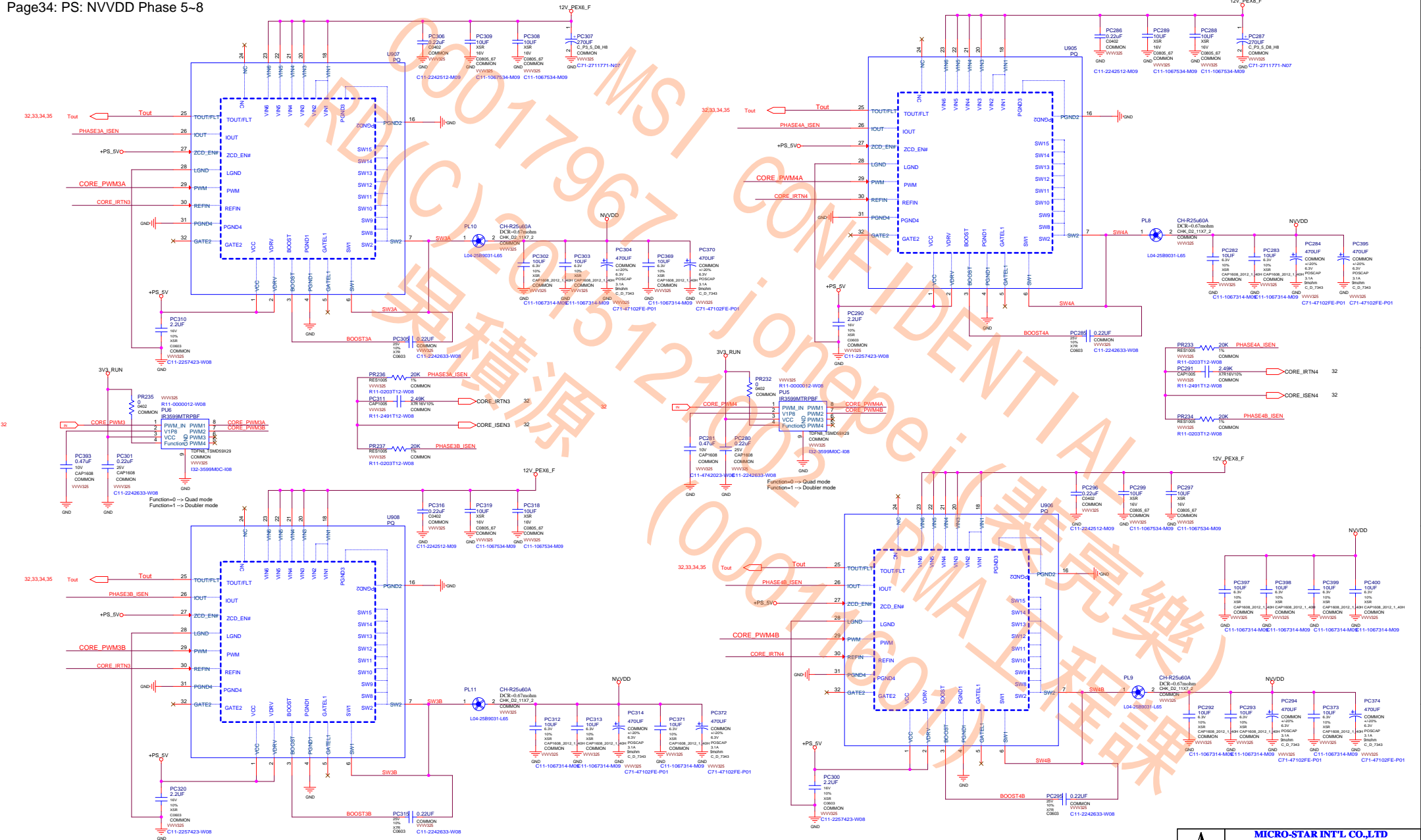
P-STATE VOLTAGES

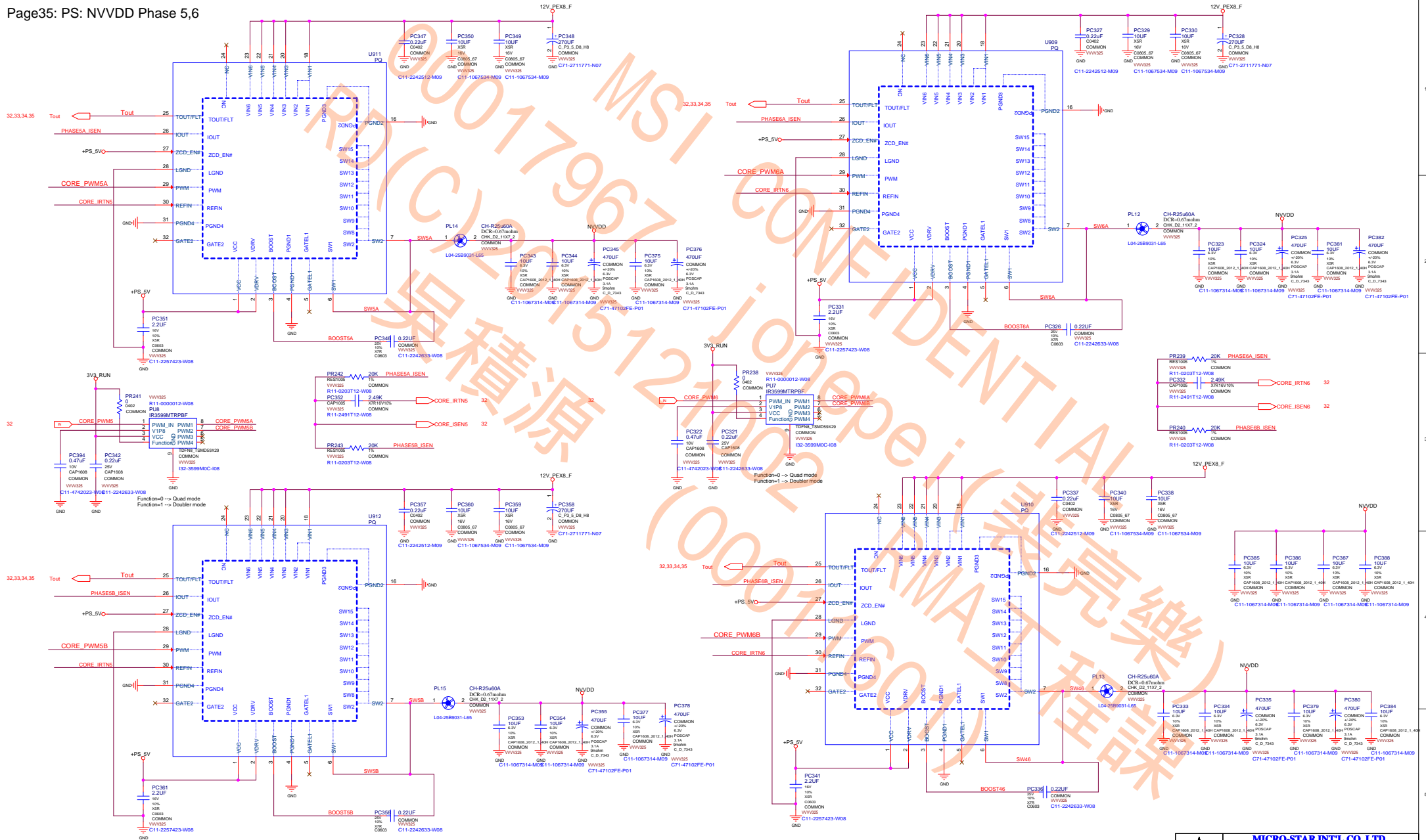
1. P0 at 1.05V to 1.15V (depending on
2. P8/P12 at 0.80V



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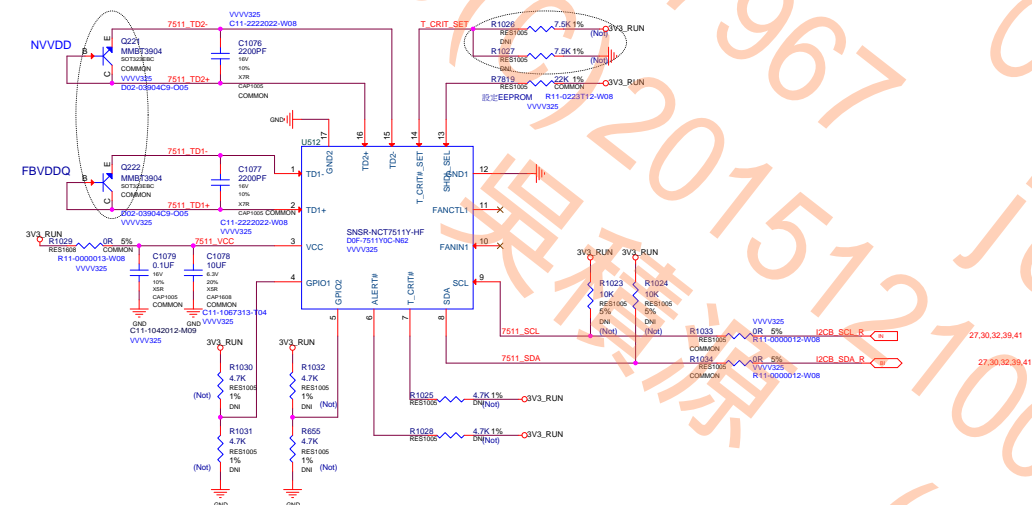
Thermal IC : NCT7511Y

Layout notice :

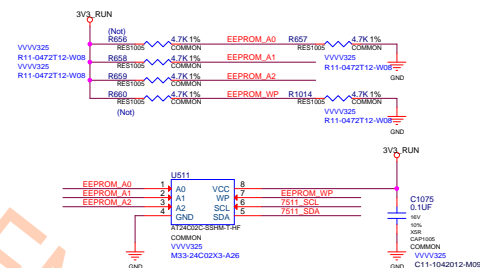
- Layout notice :
- *Add ground shielding for D+ and Dtraces.
 - *D+/D- route has to be away from the high noise area.
 - *The recommended traces width and ground shielding spacing are 10mils.

Please refer datasheet
TCRIT_SET Table
If floating, shutdown temp. set to 65°C

Thermal Diode



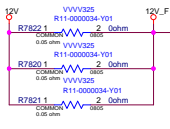
EEPROM



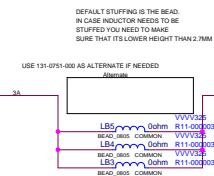
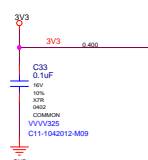
Page37: PS: Inputs, Filtering, and Monitoring

4/29 remove 12V_PEX8_VIN2 to 12V_PEX_VIN1, change and add EXT-POWER connector circuit

PEX_12V INPUT - 66W

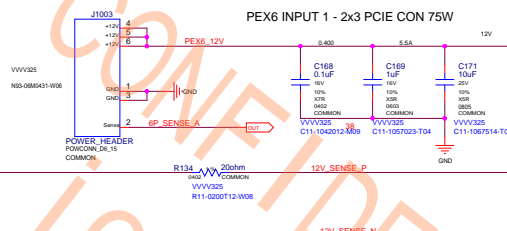


PEX 3V3 INPUT - 10W

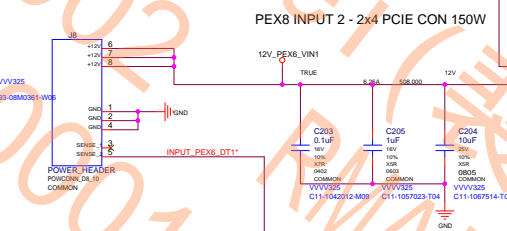


3V3_FILTER CONNECTS to 3V3_RUN.
VIA CIRCUITRY FOUND ON THE MCU PAGE.
USING EITHER THE FET LABELED Qx OR
RESISTORS LABELED Rj and Rk

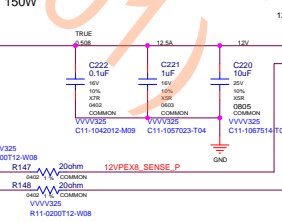
PEX6 INPUT 1 - 2x3 PCIe CON 75W



PEX8 INPUT 2 - 2x4 PCIe CON 150W



PEX8 INPUT 2 - 2x4 PCIe CON 150W

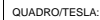


STUFF for CPU 8-PIN Power Connector



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For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



PEX 6 INPUT DETECT MUST BE DISABLED

STUFF R_{nv} IN STEERING CIRCUIT

4/30 3V3 change 3V3_RUN



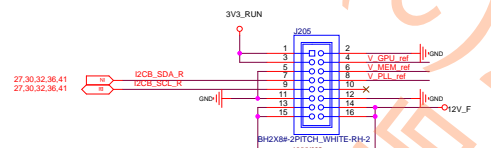
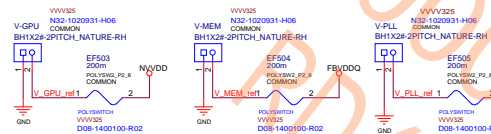
4/30 3V3 change 3V3_RUN



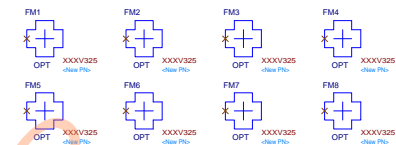
TESLA SKU:
FULL POWER WHEN 6PIN+8PIN OR 8PIN ONLY ARE PRESENT
STUFF Q508 ONLY

4/29 remove PS_NVVDD_DRVON circuit

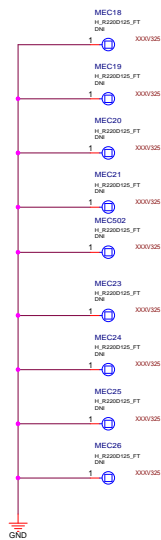
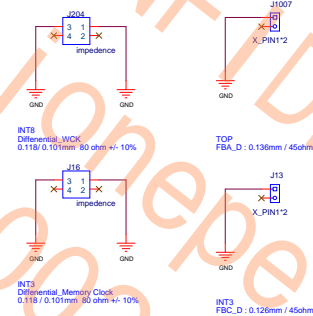




optical cross point



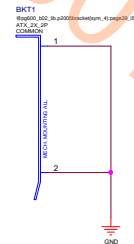
Top & bottom each layer set 4 points



Mechanical Holes Symbol



Brackets:
DIVDVL_HDMI_DP-151-10001-0441-092

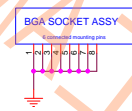


Bracket Screw

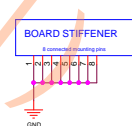
Stiffener

STIFFENER
NO PIN

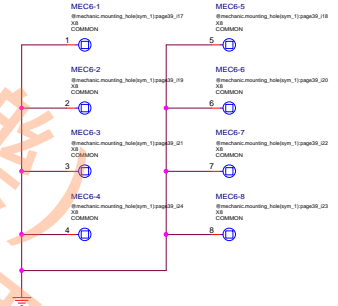
GPU SOCKET



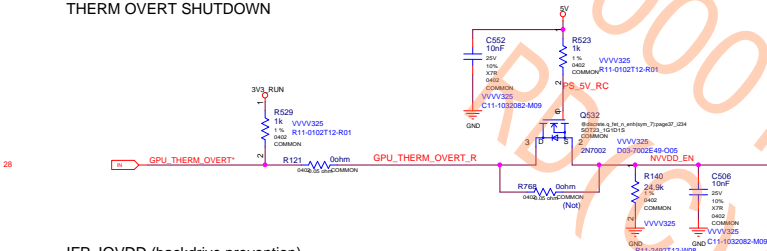
GPU Stiffener (BRING-UP COOLER)



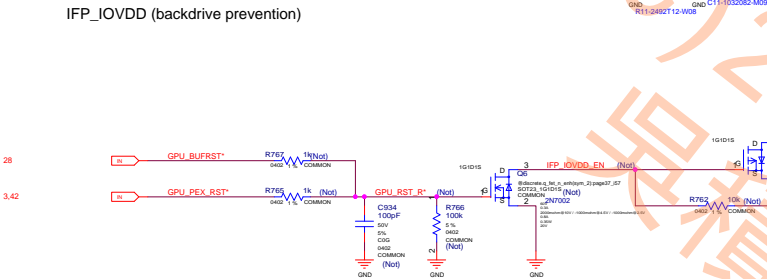
Bring Up Cooler



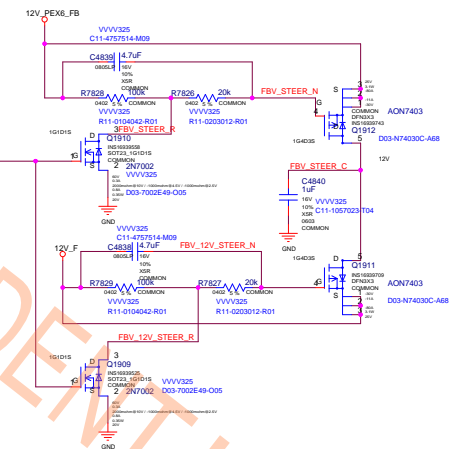
THERM OVERT SHUTDOWN

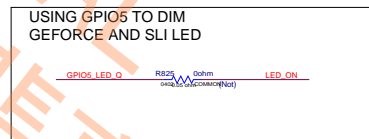
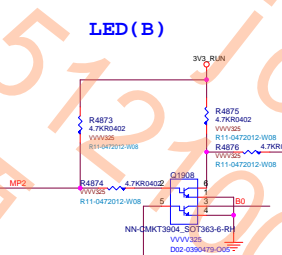
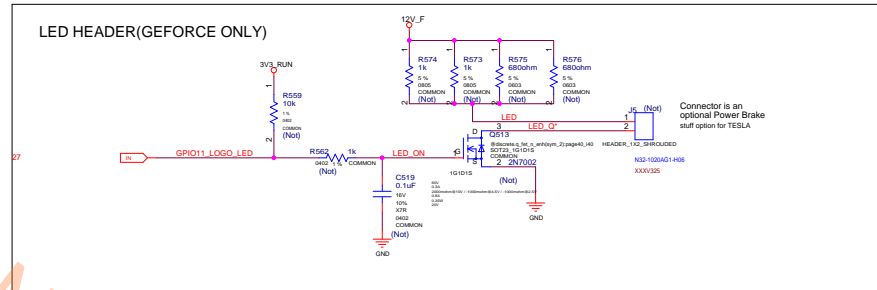


IFP_IOVDD (backdrive prevention)

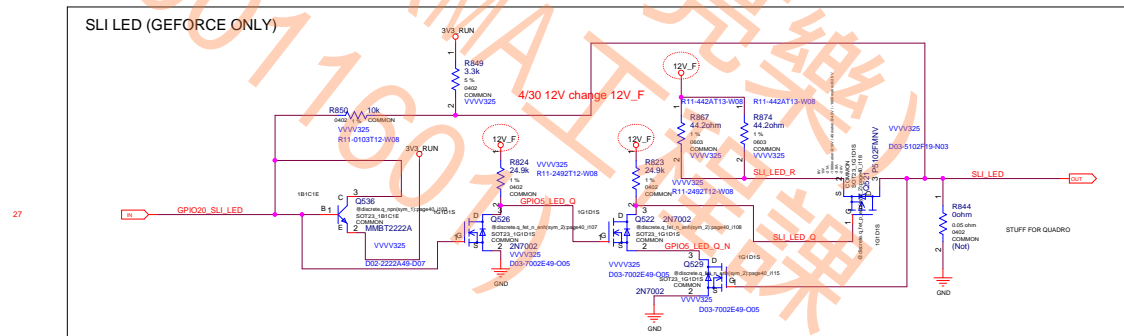


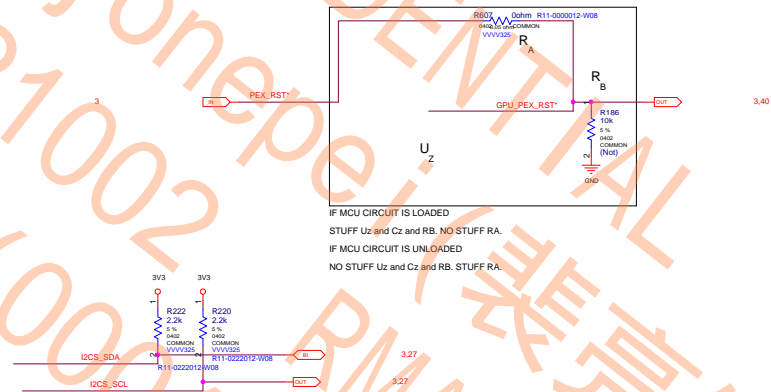
4/29 add FB 12 current steering circuit





4/289 remove



[illegible]

IF MCU CIRCUIT IS LOADED
STUFF Qx and NO STUFF Rj and Rk
IF MCU CIRCUIT IS UNLOADED
NO STUFF Qx and STUFF Rj and Rk

